Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims:

1. (canceled)

2. (new) A lateral N-channel DMOS transistor formed in a P-type semiconductor substrate, the substrate not comprising an epitaxial layer, the transistor comprising:

a field oxide layer partially covering the surface of the substrate, a first opening and a second opening being formed in the field oxide layer;

a gate overlying the substrate, a first portion of the gate being separated from the substrate in the first opening of the field oxide layer by a gate dielectric layer and a second portion of the gate stepping up over an edge of the first opening in the field oxide layer and overlying at least a portion of the field oxide layer;

an N-type source region formed at the surface of the substrate in the first opening of the field oxide layer on one side of the gate;

a P-type body region having a junction with the source region and including a channel region underlying the gate dielectric layer, the P-type body region being electrically connected to the N-type source region;

an N-type drain region located at the surface of the substrate in the second opening of the field oxide layer, the N-type drain region having a first average doping concentration of N-type dopant; and

a drift region located at least partially under the field oxide layer between the body region and the N-type drain region, the drift region having a second average doping concentration of N-type dopant;

wherein a peak doping concentration of the drift region is located below the surface of the substrate and a surface doping concentration of the drift region is lower than the peak concentration;

wherein the first doping average concentration is greater than the second doping average concentration.

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3. (new) The lateral N-channel DMOS transistor of Claim 2 wherein a depth of a portion of the drift region located beneath the N-type drain region has a deeper junction depth than a portion of the drift region located beneath the field oxide layer.

4. (new) The lateral N-channel DMOS transistor of Claim 2 where a depth of the portion of the drift region located beneath the N-type drain region has a deeper junction depth than a portion of the drift region located beneath the gate.

5. (new) The lateral N-channel DMOS transistor of Claim 2 wherein the N-type drain region abuts an N well

6. (new) The lateral N-channel DMOS transistor of Claim 2 wherein a portion of the P-type body region not located beneath the gate has a deeper junction depth than a portion of the P-type body region located beneath the gate.

7. (new) The lateral N-channel DMOS transistor of Claim 2 wherein the P-type body region comprises a P well that extends laterally to a location beneath the gate.

8. (new) A lateral P-channel DMOS formed in a P-type semiconductor substrate, the substrate not comprising an epitaxial layer, the transistor comprising:

an N-type isolation region in the substrate, the isolation region comprising a deep N-layer and a first annular N well, the first annular N well extending downward from a surface of the substrate to the deep N layer, the isolation region enclosing an isolated region of the substrate, the isolated region having a first doping concentration of P-type dopant;

a P-type source region located at the surface of the substrate within the first annular N well, a first metal contact overlying the substrate and in electrical contact with the P-type source region and the first annular N well;

a gate separated from the substrate by a gate dielectric layer and overlying a channel region of the first annular N well;

a P-type drain region at the surface of the substrate in the isolated region, the P-type drain region having a second doping concentration of P-type dopant; wherein the second doping concentration is greater than the first doping concentration; and

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a second metal contact overlying the substrate and in electrical contact with the P-type drain region.

9. (new) The lateral P-channel DMOS of Claim 8 wherein the first annular N well comprises a vertical stack of N implants.

10. (new) The lateral P-channel DMOS of Claim 8 wherein the first annular N well has a non-Gaussian vertical dopant profile.

11. (new) The lateral P-channel DMOS of Claim 8 wherein the first annular N well forms a ring or annulus laterally surrounding the isolated region.

12. (new) The lateral P-channel DMOS of Claim 8 wherein a junction avalanche breakdown voltage of the P-type drain region relative to the isolation region exceeds 20 volts.

13. (new) The lateral P-channel DMOS of Claim 8 wherein a junction avalanche breakdown voltage of the P-type drain region relative to the isolation region exceeds 30 volts.

14. (new) The lateral P-channel DMOS of Claim 8 wherein a junction avalanche breakdown voltage of the isolation region relative to a surrounding portion of the substrate not enclosed by the isolation region exceeds 20 volts.

15. (new) The lateral P-channel DMOS of Claim 8 wherein a junction avalanche breakdown voltage of the isolation region relative to a surrounding portion of the substrate not enclosed by the isolation region exceeds 30 volts.

16. (new) The lateral P-channel DMOS of Claim 8 wherein a peak dopant concentration of the deep N layer is located at a depth at least 0.5 microns below the surface of the substrate.

17. (new) A lateral trench DMOS transistor formed in a substrate of a first conductivity type, the substrate not comprising an epitaxial layer, the transistor comprising:

a trench formed at a surface of the substrate, a conductive gate material being disposed in the trench, the gate material being separated from the semiconductor substrate by a dielectric layer;

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a field oxide layer laterally spaced apart for the trench and overlying a portion of the substrate;

a source region of a second conductivity type opposite to the first conductivity type adjacent a side wall of the trench and the surface of the substrate;

a body region of the first conductivity type adjacent the source region and the side wall of the trench, the source and body regions being electrically shorted together;

a drain region of the second conductivity type adjacent the surface of the substrate and spaced apart laterally from the source region, the drain region having a first doping concentration of the second conductivity type; and

a drift region of the second conductivity type abutting the body and drain regions and the side wall of the trench, the drift region comprising a second doping concentration of the second conductivity type, the drift region comprising a shallower portion under the field oxide layer and a deeper portion not under the field oxide layer;

wherein the first doping concentration is greater than the second doping concentration.

18. (new) The lateral trench DMOS of Claim 17 wherein the drain region includes a well of the same conductivity type as the drain region, the well having a depth greater than the drift region.

19. (new) The lateral trench DMOS of Claim 17 wherein the first conductivity type is P-type and the second conductivity type is N-type.

20. (new) The lateral trench DMOS of Claim 17 wherein the body region includes a body contact region of the first conductivity type, the body contact region having a doping concentration higher than the body region.

21. (new) The lateral trench DMOS of Claim17 wherein the drift region comprises a total charge in the range of 1×10^{12} cm^{-2} to 3×10^{12} cm^{-2}.

22. (new) The lateral trench DMOS of Claim17 wherein the drift region has a peak doping concentration located at least 0.25 microns beneath the surface of the substrate.

23. (new) The lateral trench DMOS of Claim17 wherein the body region comprises a series of implants formed at differing energies and depths.

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24. (new) The lateral trench DMOS of Claim 17 wherein a doping profile taken in a vertical cross-section of the body region is non-Gaussian.

25. (new) The lateral trench DMOS of Claim 17 where the drift region underlies the entire body region.

26. (new) The lateral trench DMOS of Claim17 wherein the trench is separated laterally from the drain region by at least 3 microns.

27. (new) The lateral trench DMOS of Claim 17 wherein the trench is separated laterally from the drain region by at least 6 microns.

28. (new) The lateral trench DMOS of Claim 17 wherein a polysilicon field plate is located atop the field oxide layer.

29. (new) The lateral trench DMOS of Claim 17 wherein a junction breakdown voltage of the drain region relative to the source region exceeds 13.2V.

30. (new) The lateral trench DMOS of Claim 17 wherein a junction breakdown voltage of the drain region relative to the source region exceeds 20V.

31. (new) The lateral trench DMOS of Claim 17 wherein a junction breakdown voltage of the drain region relative to the source region exceeds 30V.

32. (new) The lateral trench DMOS of Claim 17 wherein a junction breakdown voltage of the drain region relative to the substrate exceeds 30V.

33. (new) The lateral trench DMOS of Claim 17 comprising avalanche breakdown in a region between the drain region and the P body region.

34. (new) The lateral trench DMOS of Claim17 wherein the body region is biased to a potential different from a potential of the substrate.

35. (new) The lateral trench DMOS of Claim17 wherein the gate comprises two polysilicon layers, formed from different depositions, each of the polysilicon layers being doped with material of the same conductivity type.

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36. (new) The lateral trench DMOS of Claim 17 wherein the body region comprises multiple implants formed at differing energies.

37. (new) A trench-gated MOSFET formed in a semiconductor substrate of a first conductivity type, the substrate not comprising an epitaxial layer, the trench-gated MOSFET comprising:

at least four trenches, a conductive gate material being disposed in each of the trenches, the gate material in each trench being separated from the semiconductor substrate by a dielectric layer, a first trench being separated from a second trench by a first mesa, the second trench being separated from a third trench by a second mesa, and the third trench being separated from a fourth trench by a third mesa;

the second mesa comprising:

a source region of a second conductivity type opposite to the first conductivity type adjacent a surface of the substrate, the source region having a first doping concentration of the second conductivity type;

a body region of the first conductivity type adjacent the source region and extending across the second mesa, the body region having a junction depth deeper than the source region; and

a high voltage drift region adjacent the body region and extending across the second mesa, the high voltage drift region having a second doping concentration of the second conductivity type;

each of the first and third mesas comprising:

a drain region of the second conductivity adjacent a surface of the substrate and extending entirely across the first and third mesas, respectively, the drain region having a third doping concentration of the second conductivity type; and

a well of the second conductivity type adjacent the drain region and extending entirely across the first and third mesas, respectively, the well having a fourth doping concentration of the second conductivity type; and

a layer of the second conductivity type, the layer abutting a bottom of each of the first, second, third and fourth trenches;

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wherein the first doping concentration is greater than the second doping concentration and the third doping concentration is greater than the fourth doping concentration.

38. (new) The trench-gated MOSFET of Claim 37 wherein each of the first and third mesas comprises a high voltage drift region.

39. (new) The trench-gated MOSFET of Claim 37 comprising a deep second layer of second conductivity type located beneath the layer of second conductivity type, the deep second layer having a fifth doping concentration.

40. (new) The trench-gated MOSFET of Claim 39 wherein the fifth doping concentration is greater than the fourth doping concentration.

41. (new) The trench-gated MOSFET of Claim 37 wherein the MOSFET comprises an array of cells, the cells including mesas similar to the first mesa alternating with cells similar to the second mesa, the mesas being separated by intervening trenches.

42. (new) The trench-gated MOSFET of Claim 41 wherein viewed from above the cells are polygonal.

43. (new) The trench-gated MOSFET of Claim 41 wherein viewed from above the cells are rectamgular.

44. (new) The trench-gated MOSFET of Claim 41 wherein viewed from above the cells are square.

45. (new) The trench-gated MOSFET of Claim 41 wherein viewed from above the cells are longitudinal stripes.

46. (new) The trench-gated MOSFET of Claim 41 comprising electrical contacts to respective body regions in the cells, the electrical contacts occurring in a regular and repeated spacing.

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47. (new) The trench-gated MOSFET of Claim 37. wherein the body region has a non-Gaussian doping profile in a vertical cross-section.

48. (new) The trench-gated MOSFET of Claim 37 wherein the body region comprises a series of implants formed at differing energies.

49. (new) The trench-gated MOSFET of Claim 37 wherein the body region has a peak doping concentration higher a doping concentration of first conductivity material at the surface of the substrate.

50. (new) The trench-gated MOSFET of Claim 37 wherein the gate comprises two polysilicon layers, formed from different depositions, each of the polysilicon layers being doped with material of the same conductivity type.

51. (new) The trench-gated MOSFET of Claim 37 wherein the at least four trenches are separate from each other.

52. (new) The trench-gated MOSFET of Claim 37 wherein the at least four trenches are part of an array of interconnected trenches.

53. (new) The trench-gated MOSFET of Claim 37 wherein the second mesa comprises a body contact region of the first conductivity type formed in an opening in the source region to facilitate contact to the body region, the body contact region having a sixth doping concentration, a doping concentration of the body contact region at the surface of the substrate being higher than a doping concentration of the body region.

54. (new) A trench-gated MOSFET formed in a semiconductor substrate of a first conductivity type, the substrate not comprising an epitaxial layer, the trench-gated MOSFET comprising:

at least four trenches, a conductive gate material being disposed in each of the trenches, the gate material in each trench being separated from the semiconductor substrate by a dielectric layer, a first trench being separated from a second trench by a first mesa, the second trench being separated from a third trench by a second mesa, and the third trench being separated from a fourth trench by a third mesa;

the second mesa comprising:

a source region of a second conductivity type opposite to the first conductivity type adjacent a surface of the substrate, the source region having a first doping concentration of the second conductivity type;

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a body region of the first conductivity type adjacent the source region and extending across the second mesa, the body region having a junction depth deeper than the source region; and

a high voltage drift region adjacent the body region and extending across the second mesa, the high voltage drift region having a second doping concentration of the second conductivity type;

each of the first and third mesas comprising:

a drain region of the second conductivity adjacent a surface of the substrate and extending entirely across the first and third mesas, respectively, the drain region having a third doping concentration of the second conductivity type; and

a well of the second conductivity type adjacent the drain region and extending entirely across the first and third mesas, respectively, the well having a fourth doping concentration of the second conductivity type; and

a first layer of the second conductivity type, the first layer abutting a bottom of each of the first and second trenches and the high voltage drift region; and

a second layer of the second conductivity type, the second layer abutting a bottom of each of the third and fourth trenches and the high voltage drift region, the first layer being spaced apart from the second layer;

wherein the first doping concentration is greater than the second doping concentration and the third doping concentration is greater than the fourth doping concentration.

55. (new) The trench-gated MOSFET of Claim 54 wherein each of the first and third mesas comprises a high voltage drift region.

56. (new) The trench-gated MOSFET of Claim 54 comprising a deep third layer of second conductivity type located beneath the first and second layers of second conductivity type, the deep third layer having a fifth doping concentration.

57. (new) The trench-gated MOSFET of Claim 56 wherein the fifth doping concentration is greater than the fourth doping concentration.

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58. (new) The trench-gated MOSFET of Claim 54 wherein the MOSFET comprises an array of cells, the cells including mesas similar to the first mesa alternating with cells similar to the second mesa, the mesas being separated by intervening trenches.

59. (new) The trench-gated MOSFET of Claim 58 wherein viewed from above the cells are polygonal.

60. (new) The trench-gated MOSFET of Claim 58 wherein viewed from above the cells are rectangular.

61. (new) The trench-gated MOSFET of Claim 58 wherein viewed from above the cells are square.

62. (new) The trench-gated MOSFET of Claim 58 wherein viewed from above the cells are longitudinal stripes.

63. (new) The trench-gated MOSFET of Claim 58 comprising electrical contacts to respective body regions in the cells, the electrical contacts occurring in a regular and repeated spacing.

64. (new) The trench-gated MOSFET of Claim 54 wherein the body region has a non-Gaussian doping profile in a vertical cross-section.

65. (new) The trench-gated MOSFET of Claim 54 wherein the body region comprises a series of implants formed at differing energies.

66. (new) The trench-gated MOSFET of Claim 54 wherein the body region has a peak doping concentration higher a doping concentration of first conductivity material at the surface of the substrate.

67. (new) The trench-gated MOSFET of Claim 54 wherein the gate comprises two polysilicon layers, formed from different depositions, each of the polysilicon layers being doped with material of the same conductivity type.

68. (new) The trench-gated MOSFET of Claim 54 wherein the at least four trenches are part of an array of interconnected trenches.

69. (new) The trench-gated MOSFET of Claim 54 wherein the at least four trenches are part of an array of interconnected trenches.

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70. (new) The trench-gated MOSFET of Claim 54 wherein the second mesa comprises a body contact region of the first conductivity type formed in an opening in the source region to facilitate contact to the body region, the body contact region having a sixth doping concentration, a doping concentration of the body contact region at the surface of the substrate being higher than a doping concentration of the body region.

71. (new) A trench-gated MOSFET formed in a semiconductor substrate of a first conductivity type, the substrate not comprising an epitaxial layer, the trench-gated MOSFET comprising:

at least four trenches formed at a surface of the substrate, the gate material in each trench being separated from the semiconductor substrate by a dielectric layer, a first trench being separated from a second trench by a first mesa, the second trench being separated from a third trench by a second mesa, and the third trench being separated from a fourth trench by a third mesa;

the first mesa comprising:

a drain region of a second conductivity opposite to the first conductivity type adjacent a surface of the substrate and extending across the first mesa, the drain region having a first doping concentration of the second conductivity type; and

a well of the second conductivity type adjacent the drain region and extending across the first mesa, the well having a second doping concentration of the second conductivity type;

each of the second and third mesas comprising:

a source region of the second conductivity type adjacent a surface of the substrate, the source region having a third doping concentration of the second conductivity type;

a body region of the first conductivity type adjacent the source region and extending across the second and third mesas, respectively, the body region having a junction depth deeper than the source region; and

a high voltage drift region adjacent the body region and extending across the second mesa, the high voltage drift region having a second doping concentration of the second conductivity type;

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a layer of the second conductivity type, the layer abutting a bottom of each of the first, second, third and fourth trenches;

wherein the first doping concentration is greater than the second doping concentration and the third doping concentration is greater than the fourth doping concentration.

72. (new) The trench-gated MOSFET of Claim 71 wherein the first mesa comprises a high voltage drift region.

73. (new) The trench-gated MOSFET of Claim 71 comprising a deep second layer of second conductivity type located beneath the layer of second conductivity type, the deep second layer having a fifth doping concentration.

74. (new) The trench-gated MOSFET of Claim 73 wherein the fifth doping concentration is greater than the fourth doping concentration.

75. (new) The trench-gated MOSFET of Claim 71 wherein the MOSFET comprises an array of cells, the cells including mesas similar to the first mesa alternating with cells similar to the second mesa, the mesas being separated by intervening trenches.

76. (new) The trench-gated MOSFET of Claim 75 wherein viewed from above the cells are polygonal.

77. (new) The trench-gated MOSFET of Claim 75 wherein viewed from above the cells are rectangular.

78. (new) The trench-gated MOSFET of Claim 75 wherein viewed from above the cells are square.

79. (new) The trench-gated MOSFET of Claim 75 wherein viewed from above the cells are longitudinal stripes.

80. (new) The trench-gated MOSFET of Claim 75 comprising electrical contacts to respective body regions in the cells, the electrical contacts occurring in a regular and repeated spacing.

81. (new) The trench-gated MOSFET of Claim 71 wherein the body region has a non-Gaussian doping profile in a vertical cross-section.

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82. (new) The trench-gated MOSFET of Claim 71 wherein the body region comprises a series of implants formed at differing energies.

83. (new) The trench-gated MOSFET of Claim 71 wherein the body region has a peak doping concentration higher a doping concentration of first conductivity material at the surface of the substrate.

84. (new) The trench-gated MOSFET of Claim 71 wherein the gate comprises two polysilicon layers, formed from different depositions, each of the polysilicon layers being doped with material of the same conductivity type.

85. (new) The trench-gated MOSFET of Claim 71 wherein the at least four trenches are part of an array of interconnected trenches.

86. (new) The trench-gated MOSFET of Claim 71 wherein the at least four trenches are part of an array of interconnected trenches.

87. (new) The trench-gated MOSFET of Claim 71 wherein each of the second and third mesas comprises a body contact region of the first conductivity type formed in an opening in the source region to facilitate contact to the body region, the body contact region having a sixth doping concentration, a doping concentration of the body contact region at the surface of the substrate being higher than a doping concentration of the body region.

88. (new) A trench-gated MOSFET formed in a semiconductor substrate of a first conductivity type, the substrate not comprising an epitaxial layer, the trench-gated MOSFET comprising:

an array of trenches formed at a surface of the substrate, the trenches forming and defining plurality of mesas, the plurality of mesas including source mesas and drain mesas;

each trench holding a conductive gate material, the gate material in each trench being separated from the substrate by a dielectric layer, and

each drain mesa comprising a column of dopant of the second conductivity type substantially laterally contained by the trenches surrounding the drain mesa, and

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each source mesa comprising a three-layer sandwich of alternately doped layers including an upper layer doped with a dopant of the second conductivity type, the upper layer being adjacent the surface of the substrate and acting as a source region, a middle layer doped with a dopant of the first conductivity type, the middle layer acting as a body/channel region, an opening being formed in the upper layer, the opening extending from the surface of the substrate to the middle layer and being filled with a dopant of the first conductivity type to facilitate the biasing of the body/channel region, and a lower layer doped with a dopant of the second conductivity type, the lower layer acting as a drain region, the dopants in the three-layer sandwich being substantially laterally contained by the trenches surrounding the source mesa,

a deep drain layer of the second conductivity type extending beneath the source and drain mesas and having a bottom junction depth deeper than the trenches, wherein the deep drain layer overlaps and is electrically shorted to the column of dopant of the second conductivity type in each of the drain mesas; and to the lower layer in each of the source mesas;

an electrical contact to the column of dopant of second conductivity type in each of the drain mesas;

an electrical contact to the upper layer and the dopant of first conductivity type in the opening in the upper layer in each of the source mesas; and

an electrical contact to the conductive gate material in the trenches.

89. (new) The trench-gated MOSFET of Claim 88 wherein the trenches form an orthogonal grid that separates the source and drain mesas.

90. (new) The trench-gated MOSFET of Claim 88 wherein the mesas are formed into a pattern of cells, each cell including only a single drain mesa and a plurality of source mesas.

91. (new) The trench-gated MOSFET of Claim 88 wherein viewed from above the source and drain mesas are in the form of longitudinal stripes.

92. (new) The trench-gated MOSFET of Claim 88 wherein viewed from above the source and drain mesas are rectangular.

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93. (new) The trench-gated MOSFET of Claim 88 wherein viewed from above the source and drain mesas are square.

94. (new) The trench-gated MOSFET of Claim 88 wherein viewed from above the source and drain mesas are polygonal.

95. (new) The trench-gated MOSFET of Claim 88 wherein the deep drain layer is formed by ion implantation.

96. (new) The trench-gated MOSFET of Claim 88 wherein the deep drain layer has a peak doping concentration at a level deeper than a level of a bottom of the trenches.

97. (new) The trench-gated MOSFET of Claim 88 wherein the deep drain layer has a peak doping concentration higher than a doping concentration of second conductivity type at the surface of the substrate.

98. (new) The trench-gated MOSFET of Claim 88 wherein the column of dopant of the second conductivity type in each drain mesa comprises multiple implants performed at differing energies.

99. (new) The trench-gated MOSFET of Claim 88 wherein the lower layer in each of the source mesas is formed by a high energy ion implantation.

100. (new) The trench-gated MOSFET of Claim 88 wherein the three-layer sandwich in each source mesa is formed by multiple implants performed at differing energies.

101. (new) The trench-gated MOSFET of Claim 88 wherein middle layer of the three-layer sandwich in each source mesa is formed by multiple implants performed at differing energies.

102. (new) A family of semiconductor devices formed in a semiconductor substrate of a first conductivity type, the substrate not comprising an epitaxial layer, the family comprising:

a lateral trench DMOS transistor comprising:

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a first trench formed at a surface of the substrate, a conductive gate material being disposed in the first trench, the gate material being separated from the semiconductor substrate by a first dielectric layer;

a source region of a second conductivity type opposite to the first conductivity type adjacent a side wall of the first trench and the surface of the substrate;

a body region of the first conductivity type adjacent the source region and the side wall of the first trench, the source and body regions being electrically shorted together;

a drain region of the second conductivity type adjacent the surface of the substrate and spaced apart laterally from the source region, the drain region having a first doping concentration of the second conductivity type; and

a drift region of the second conductivity type abutting the body and drain regions and the side wall of the first trench, the drift region comprising a second doping concentration of the second conductivity type;

wherein the first doping concentration is greater than the second doping concentration; and

a quasi-vertical trench-gated MOSFET comprising:

an array of second trenches formed at a surface of the substrate, the second trenches forming and defining plurality of mesas, the plurality of mesas including source mesas and drain mesas;

each second trench holding a conductive gate material, the gate material in each second trench being separated from the substrate by a second dielectric layer, and

each drain mesa comprising a column of dopant of the second conductivity type substantially laterally contained by the second trenches surrounding the drain mesa, and

each source mesa comprising a three-layer sandwich of alternately doped layers including an upper layer doped with a dopant of the second conductivity type, the upper layer being adjacent the surface of the substrate

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and acting as a source region, a middle layer doped with a dopant of the first conductivity type, the middle layer acting as a body/channel region, an opening being formed in the upper layer, the opening extending from the surface of the substrate to the middle layer and being filled with a dopant of the first conductivity type to facilitate the biasing of the body/channel region, and a lower layer doped with a dopant of the second conductivity type, the lower layer acting as a drain region, the dopants in the three-layer sandwich being substantially laterally contained by the second trenches surrounding the source mesa,

a deep drain layer of the second conductivity type extending beneath the source and drain mesas and having a bottom junction depth deeper than the second trenches, wherein the deep drain layer overlaps and is electrically shorted to the column of dopant of the second conductivity type in each of the drain mesas; and to the lower layer in each of the source mesas;

wherein the first trench and the array of second trenches are formed in a single sequence of process steps.

103. (new) A family of semiconductor devices formed in a P-type semiconductor substrate, the substrate not comprising an epitaxial layer, the family comprising:

a quasi-vertical trench-gated MOSFET comprising:

an array of trenches formed at a surface of the substrate, the trenches forming and defining plurality of mesas, the plurality of mesas including source mesas and drain mesas;

each trench holding a conductive gate material, the gate material in each trench being separated from the substrate by a dielectric layer, and

each drain mesa comprising a column of N-type dopant substantially laterally contained by the trenches surrounding the drain mesa, and

each source mesa comprising a three-layer sandwich of alternately doped layers including an upper layer doped with an N-type dopant, the upper layer being adjacent the surface of the substrate and acting as a source region, a middle layer doped with a P-type dopant, the middle layer acting as a body/channel region, an opening being formed in the upper layer,

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the opening extending from the surface of the substrate to the middle layer and being filled with a P-type dopant to facilitate the biasing of the body/channel region, and a lower layer doped with an N-type dopant, the lower layer acting as a drain region, the dopants in the three-layer sandwich being substantially laterally contained by the trenches surrounding the source mesa, and

an N drain layer extending beneath the source and drain mesas and having a bottom junction depth deeper than the trenches, wherein the N drain layer overlaps and is electrically shorted to the column of N-type dopant in each of the drain mesas; and to the lower layer in each of the source mesas; and

a PMOS comprising:

an N well having a relatively deep central portion and relatively shallow side portions, the relatively shallow side portions underlying a field oxide layer, the relatively deep central portion underlying an opening in the field oxide layer;

a second gate overlying the surface of the substrate and separated from the substrate by a second gate dielectric layer;

a P-type source region located at the surface of the substrate in the N well on one side of the second gate; and

a P-type drain region located at the surface of the substrate in the N well on an opposite the of the second gate from the P-type source region;

wherein the N drain layer extends to a location below the N well so as to assist in isolating the PMOS from a portion of the substrate outside the N well.

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